Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	19597	memory adj control	USPAT	OR	OFF	2004/11/03 13:55
L2	236330	power adj supply	USPAT	OR	OFF	2004/11/03 13:55
L3	213	l1 with l2	USPAT	OR	OFF	2004/11/03 13:55
L5	25	l3 with battery	USPAT	OR	OFF	2004/11/03 13:58
L6	1	l5 with self$1refresh	USPAT	OR	OFF	2004/11/03 14:30
L9	341	pull$1 adj down adj resistance	USPAT; JPO	OR	OFF	2004/11/03 14:32
L10	15	l9 with memory	USPAT; JPO	OR	OFF	2004/11/03 14:38
L11	120018	power adj4 (sav$3 down failure shut off cut)	USPAT; JPO	OR	OFF	2004/11/03 14:44
L12	10003	l11 with (controller cpu processor)	USPAT; JPO	OR	OFF	2004/11/03 14:45
L13	1732	l12 with (memory ram dram)	USPAT; JPO	OR	OFF	2004/11/03 14:46
L14	232	l13 with battery	USPAT; JPO	OR	OFF	2004/11/03 15:07
L16	12	l14 with refresh	USPAT; JPO	OR	OFF	2004/11/03 14:47
L27	41205	("365").CLAS.	USPAT; USOCR	OR	OFF	2004/11/03 15:09
L28	846	(365/228,229).CCLS.	USPAT; USOCR	OR	OFF	2004/11/03 15:10
L31	228	l28 and resistance	USPAT	OR	OFF	2004/11/03 15:11
L32	212	l31 and memory	USPAT	OR	OFF	2004/11/03 15:12
L33	180	l32 and switch$3	USPAT	OR	OFF	2004/11/03 15:12
L34	98	l33 and battery	USPAT	OR	OFF	2004/11/03 15:12
L35	27	l34 and refresh	USPAT	OR	OFF	2004/11/03 15:13